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VDTA BASED GROUNDED TO FLOATING ADMITTANCE ELECTRONICALLY CONVERTER

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Abstract

In this article, a new grounded to floating admittance convertor employing only two voltage differencing transconductance amplifiers (VDTAs) has been suggested. The proposed configuration is able to convert any arbitrary grounded admittance into floating admittance without any requirement of additional passive element. The equivalent floating admittance value can tuned electronically through VDTA transconductance. Depending on the passive element selection, the presented topology can simulate active floating resistor and floating capacitor. The presented circuit does not require any active/passive component matching constraints; it has low sensitivity values and good non-ideal behavior. The influence of VDTA port parasitic on proposed configuration is also investigated. The validity of proposed circuit is verified by some application examples. VDTA based Grounded to Floating Admittance converter is implemented & simulated with PSPICE using the 0.18um CMOS technology.

Keywords:

Floating Admittance, VDTA, Electronic Control, No Matching Constraints

1. INTRODUCTION

Active simulation of admittance functions is a popular research area for analog circuit designers and researchers as these simulators can be used in design of active filters, oscillators and cancellation of parasitic. The realization of floating admittance function simulator is always more difficult than the grounded simulator due to limitations of integrated circuit technology. So, several grounded to floating admittance convertor has been proposed in literature which can convert a grounded admittance into a floating admittance with some multiplication factor. These circuits can be used to simulate floating resistors, capacitors, inductors and frequency dependent negative resistors (FDNRs) by proper selection of components. Several such simulators employing different active elements such as current conveyors, current backward transconductance amplifier (CBTA), current follower transconductance amplifiers (CFTA) and differential voltage second generation current conveyor (DVCCII) have been reported in literature. The CCCII based simulator circuit has been proposed in [1], which employs four CCCII and able to convert a grounded admittance into floating one. This circuit can be viewed as a purely active circuit as it does not need any additional admittance except the one need to for conversion. The configuration proposed in [2] has two DO-CCIIs along with three admittances (two grounded and one floating) out of which one of the grounded admittance is converted into floating form. This configuration has drawbacks like use of external admittances and lack of electronic control. The circuit proposed in [3] is also a CCII based circuit with three CCII and three admittances (two grounded and one floating). The circuit proposed in [4] is an electronically tunable circuit with two CBTAs but not a purely active configuration with requirement of additional passive elements. One more CBTA based circuit has been proposed in [5] but it is also not a purely active circuit. The circuit given in [6] is purely active but requires excessive number of active elements (four CFTAs). In [7], a DVCC based circuit is proposed with non-availability of electronic tuning and presence of additional grounded admittances. The configuration proposed in [8] needs three CCII, one DVCC along with five grounded admittance. Hence this circuit has excessive active/passive component requirements. These proposed simulators can be used to realize floating resistor/capacitors/inductors and FDNRs by proper choice of passive elements.

Therefore, the aim of this paper is to propose a new grounded to floating admittance convertor employing only two VDTAs and one grounded admittance. This circuit converts the used grounded admittance into a floating admittance with electronically tunable multiplication factor. Hence, the convertor circuit can be viewed as a purely active simulator. The proposed realization exhibit following advantageous features; (i) no requirement of any additional admittance, (ii) electronically tunable multiplication factor, (iii) no requirement of any matching constraint, (iv) good non- ideal behavior and (v) low active and passive sensitivities.

2. VOLTAGE DIFFERENCING TRANSCONDUCTANCE AMPLIFIER

The VDTA is a new generation active block which has two voltage inputs and three current outputs [9]. The symbol of VDTA is shown in Fig.1 and its CMOS implementation is shown in Fig.1 [10], where the input terminals are denoted as VP and VN and output terminals are *Z*, *X*+ and *X*-.

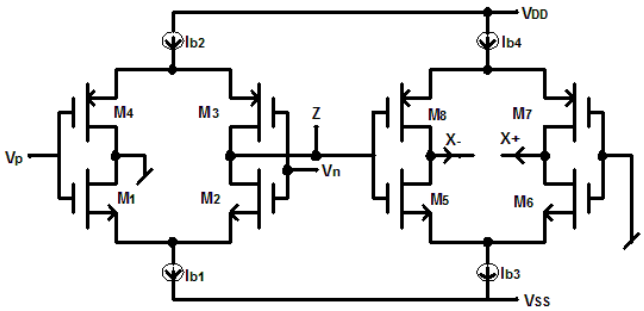

Fig.1. Voltage Difference Transconductance amplifier CMOS Implementation

Using standard notation, the terminals relationship of an ideal VDTA can be defined by

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m_1} & -g_{m_1} & 0 \\ 0 & 0 & g_{m_2} \\ 0 & 0 & -g_{m_2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad (1)$$

where,

$$g_{m_1} = \frac{g_3 + g_4}{2} \quad (2)$$

$$g_{m_2} = \frac{g_5 + g_8}{2} \text{ or } g_{m_2} = \frac{g_6 + g_7}{2} \quad (3)$$

where, g_n is the transconductance of n^{th} MOS transistor given as,

$$g_n = \sqrt{I_{B_n} \mu_n C_{OX} \left(\frac{W}{L}\right)_n} \quad (4)$$

3. THE PROPOSED CONFIGURATION

The proposed purely active grounded to floating admittance convertor is shown in Fig.2.

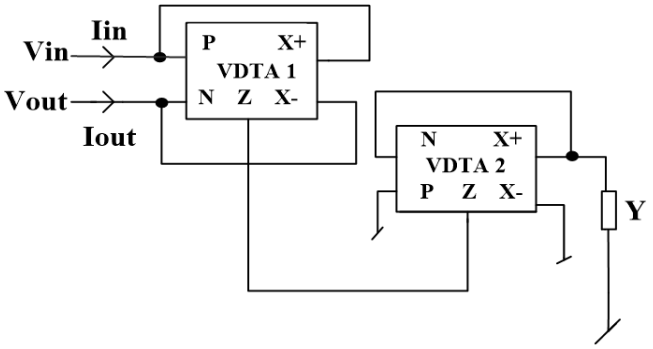

Fig.2. Proposed Configuration

By routine circuit analysis the short circuit admittance matrix can be given as,

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{g_{m_3} g_{m_4}} Y \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (5)$$

which simulate a floating admittance with admittance value,

$$Y_f = \frac{g_{m_1} g_{m_2}}{g_{m_3} g_{m_4}} Y \quad (6)$$

So, the circuit shown in Fig.3 is converting a grounded admittance Y into a floating admittance Y_f with a multiplication factor "K",

$$K = \frac{g_{m_1} g_{m_2}}{g_{m_3} g_{m_4}} \quad (7)$$

From Eq.(6), it is clear that the inductance value can be tuned electronically by changing the transconductance of VDTAs [18] [19]. The proposed configuration can be used to simulate floating resistance and floating capacitance by proper selection of Y.

I. If $Y = sC_0$ is selected, the short circuit admittance matrix is given by,

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{g_{m_3} g_{m_4}} sC_0 \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (8)$$

which simulate a floating capacitor with capacitance value,

$$C_f = \frac{g_{m_1} g_{m_2}}{g_{m_3} g_{m_4}} C_0 \quad (9)$$

II. If $Y = 1/R_0$ is selected, the short circuit admittance matrix is given by,

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{g_{m_3} g_{m_4} R_0} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (10)$$

which simulate a floating resistor with resistance value,

$$R_f = \frac{g_{m_3} g_{m_4}}{g_{m_1} g_{m_2}} R_0 \quad (11)$$

4. NON IDEAL ANALYSIS

Taking the non-ideal errors of CMOS VDTA into consideration the port relationship between various current and voltage of a VDTA can be written as [17],

$$I_Z = \beta_Z g_{m_1} \left(V_P - V_N\right) \quad (12)$$

$$I_{X+} = \beta_{x+} g_{m_2} V_Z \quad (13)$$

$$I_{X-} = -\beta_{x-} g_{m_2} V_Z \quad (14)$$

where, β_Z, β_X^+ and β_X^- are non-ideal transconductance gain errors.

On revisiting the proposed configuration under non-ideal conditions [16], the short circuit admittance matrix can be found as,

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} sC_{p1} + \frac{1}{R_{x1}} + \beta_x^+ \frac{g_{m1} g_{m2}}{a} & \beta_x^+ \frac{g_{m1} g_{m2}}{a} \\ \beta_x^- \frac{g_{m1} g_{m2}}{a} & \frac{1}{R_{x1}} + sC_{n1} + \beta_x^- \frac{g_{m1} g_{m2}}{a} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (15)$$

where,

$$a = \frac{1}{\frac{1}{R_{x2}} + \frac{1}{R_{z2}} + sC_{z1} + sC_{z2} + \frac{\beta_x^+ g_{m3} g_{m4}}{sC_0 + sC_{n2} + \frac{1}{R_{x2}}}} \quad (16)$$

5. EFFECTS OF PARASITICS

At high frequency, the terminal parasitic of VDTA comes into the picture and effect the performance of a VDTA based circuit. To study the effects of terminal parasitic of VDTAs on proposed resistance simulation configuration, it was examined including port parasitic of VDTA [11] [12] [13] [14] [15]. The Fig.3 shows the proposed convertor with port parasitic of VDTA-1 and VDTA-2. The short circuit admittance matrix taking VDTA terminal parasitic under consideration can be found as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} sC_{p1} + \frac{1}{R_{x1}} + \frac{g_{m1}g_{m2}}{a} & \frac{g_{m1}g_{m2}}{a} \\ \frac{g_{m1}g_{m2}}{a} & \frac{1}{R_{x1}} + sC_{n1} + \frac{g_{m1}g_{m2}}{a} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (17)$$

where,

$$a = \frac{1}{\frac{1}{R_{x2}} + \frac{1}{R_{z2}} + sC_{z1} + sC_{z2} + \frac{g_{m3}g_{m4}}{sC_0 + sC_{n2} + \frac{1}{R_{x2}}}} \quad (18)$$

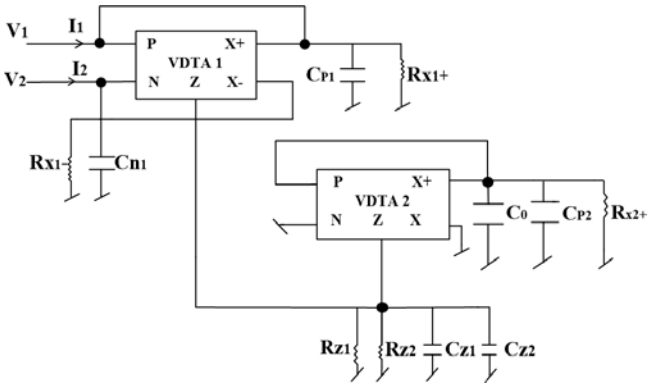

Fig.3. Proposed configuration with VDTA port parasitic

6. RESULTS

The circuit illustrated in Fig.3 (with $Y = 1/R_0$ and $R_0 = 1\text{k}\Omega$) is tested by SPICE simulations with TSMC 0.18µm process parameter model. The simulations were performed employing CMOS VDTA (shown in Fig.2) with supply voltages ±0.9 VDC and bias currents $I_{b1} = I_{b2} = I_{b3} = I_{b4} = I_{b5} = I_{b6} = I_{b7} = I_{b8} = 150\mu\text{A}$. I_{b1}, I_{b2}, I_{b3} and I_{b4} are the bias currents of VDTA1 and I_{b5}, I_{b6}, I_{b7} and I_{b8} are the bias currents of VDTA2. The magnitude response of impedance of proposed simulator has been shown in Fig.4. It is seen from Fig.4 that simulated magnitude response is constant up to 36.3MHz frequency. The phase responses, as shown in Fig.5 clearly indicate that simulated phase value is 900 up to 4.32MHz frequency. So, it can be concluded that the configuration is working as a floating resistor with resistance value of 1.64kΩ. The electronic tunability can be demonstrated by simulating it with different values of bias currents [20]. To demonstrate the electronic control of proposed configuration, simulations have been performed for different set of bias currents. The Fig.6 illustrated the magnitude responses for $I_b = 100\mu\text{A}$ and 50µA.

The proposed configuration is also simulated for $Y = sC_0$ where $C_0 = 0.1\text{nF}$ and bias currents $I_{b1} = I_{b2} = I_{b3} = I_{b4} = I_{b5} = I_{b6} = I_{b7} = I_{b8} = 150\mu\text{A}$. The simulated magnitude and phase responses illustrated in Fig.7 and Fig.8 confirm the working of the circuit as a floating capacitor. The low-pass filter is also simulated using CMOS VDTA with supply voltage of ±0.9 VDC. The value of $C_0 = 0.1\text{nF}$ and $R_0 = 1\text{k}\Omega$. The SPICE simulated frequency responses of this filters is shown in Fig.9.

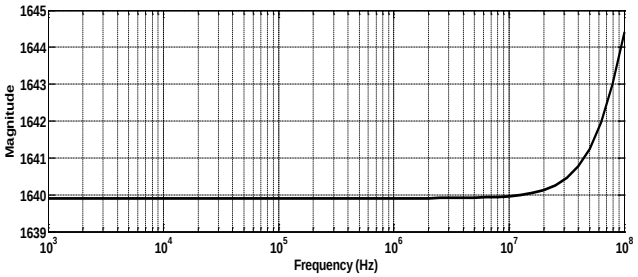

Fig.4. Magnitude Response (for $Y = 1/R_0$)

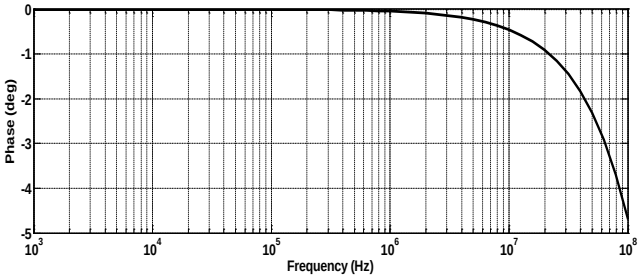

Fig.5. Phase Response (for $Y = 1/R_0$)

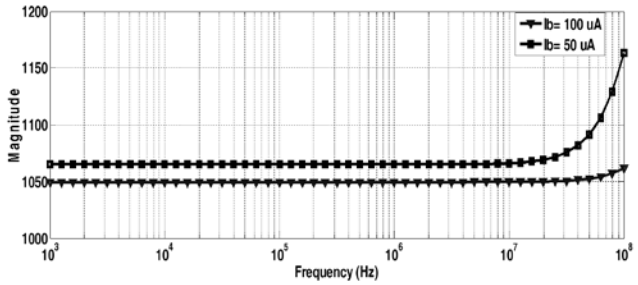

Fig.6. Magnitude responses at different bias current (for $Y = 1$)

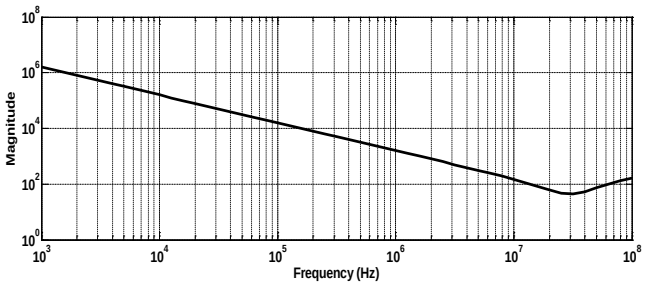

Fig.7. Magnitude Response (for $Y = sC_0$)

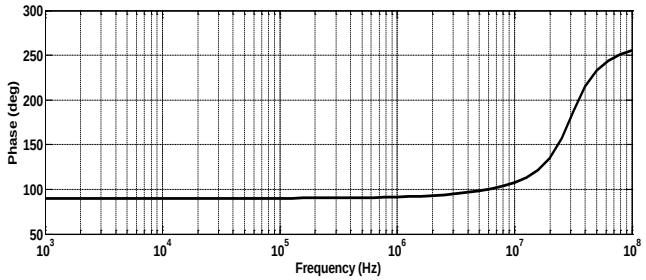

Fig.8. Phase Response (for $Y = sC_0$)

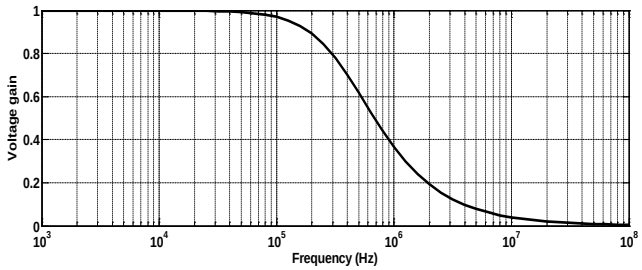

Fig.9. Frequency response of low-pass filter

7. CONCLUSION

In this paper, we have proposed new purely active floating resistor employing two VDTAs which uses supply voltages ±0.9V, thus circuit is suitable for low voltage applications. The proposed configuration uses electronically tunable resistance by control of four parameters: g_{m1}, g_{m2}, g_{m3} and g_{m4}, with low sensitivity indexes. The usefulness of proposed circuit demonstrated on filter deign example. The workability of the proposed circuits has been tested using SPICE simulations with TSMC 0.18µm CMOS process parameters.

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