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A NOVEL FINFET BASED APPROACH FOR THE REALIZATION OF TERNARY GATES

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Abstract

The Scaling of conventional Complementary Metal Oxide Semiconductors (CMOSs) has been facing problems such as short channel effect due to hot electron effect and leakage power. Fin Field Effect Transistor (FinFET) is considered as solution to this issue. Binary system occupies large area there for the circuit complexity is increasing on a VLSI chip and thus degrading the performance of binary system. Multi valued logic MVL is considered as solution to this issue. In this paper, to minimize short channel effect and reduce circuit complexity on a VLSI chip I have designed FinFET based ternary basic gates (T-NOT, ST-NAND, ST-NOR, ST-AND and ST-OR). FinFET is classified in to two types based on gate structure: 1) Short Gate FinFET (SG-FinFET) and 2) Independent Gate FinFET (IG-FinFET). The proposed ternary logic gates are design using SG-FinFET. Simulation is performed with Tanner EDA tool. The proposed design has achieved good reduction in the circuit element count.

Keywords:

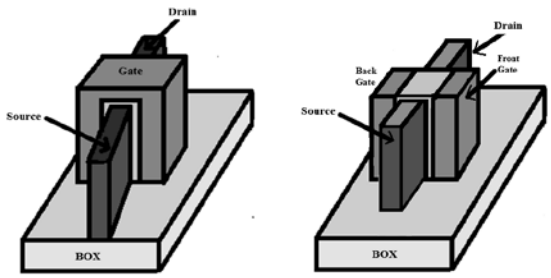
Fin Field Effect Transistor, Multi Valued Logic, Multi Valued Logic Gates, Ternary Gates

1. INTRODUCTION

Multi valued logic (MVL) circuits have a high potential for improving present day very large scale integration (VLSI) circuit designs [1]. In MVL, each wire can transmit more information than a binary element. As a result, the number of connections inside the chip can be reduced. There are two types of operation mode in MVL: 1) Voltage mode operation and 2) Current mode operation. The voltage mode operation is also classified in to two types: 1) unbalanced mode and 2) Balanced mode. In unbalanced mode operation and balanced mode operation, three voltage levels with logic value mentioned in Table.1 and Table.2, respectively. In this proposed work, I have design all gates using unbalanced mode operation i.e. voltage level V_{DD} = 0.9V, V_{DD}/2= 0.45V and Ground = 0V.

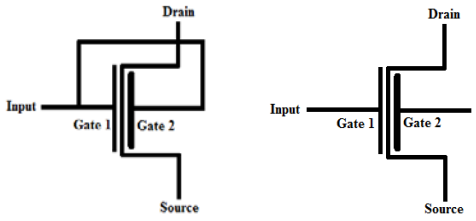
FinFET has been considered as one of the best substitutes for planar CMOS technology in the sub-32 nm regime [2]. FinFET Device has Two Different Structures a) Short Gate FinFET (SG-FinFET) and b) Independent Gate FinFET (IG-FinFET). In SG-FinFET device, top part of the gate is shorted and in IG-FinFET both gate are independent of each other which are known as front gate and back gate [2]. 3D View of SG-FinFET structure and IG-FinFET structure is shown in Fig.1(a) and Fig.1(b), respectively. The symbol of SG-FinFET and IG-FinFET is shown in Fig.2(a) and Fig.2(b), respectively. Netlist of the proposed ternary logic gates are designed with help of Berkeley BSIM4 SOI v4.0 library files for 32 nm technology using TSPICE.

The remaining part of this paper is classified as follows. Section 2 describes design of a three types of ternary inverters. Section 3 represents design of standard T-NAND gate with truth table and simulation waveforms. Section 4 represents design of standard T-NOR gate with truth table and simulation waveforms. Section 5 represents design of standard T-AND gate with truth table and simulation waveforms. Section 6 represents design of standard T-OR gate with truth table and simulation waveform. Section 8 concludes the proposed design.



(a) (b)

Fig.1. (a) SG-FinFET device structure (b) IG-FinFET device structure



(a) (b)

Fig.2. (a) Symbol of SG-FinFET (b) Symbol of IG-FinFET

Table.1. Unbalanced Mode Operation

Voltage Level	Logic Level	Voltage Level (V)
Ground	0	0
½ V_{DD}	1	0.45
V_{DD}	2	0.9

Table.2. Balanced Mode Operation

Voltage Mode	Logic Level
-V	-1
Ground	0
+V	1

2. DESIGN OF TERNARY INVERTER

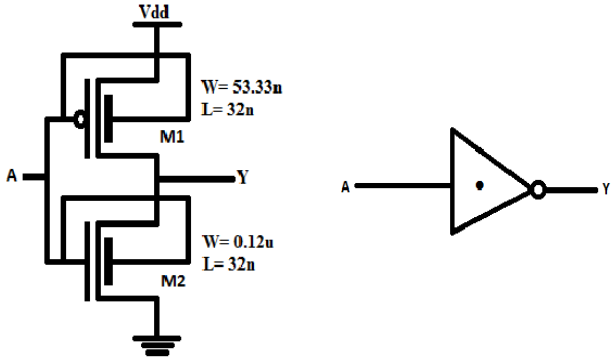
The Ternary Inverters are further classified based on the output obtained for corresponding input levels [3]. Ternary Inverters are classified in to three types of Inverters: 1) Standard Ternary Inverter (STI), 2) Positive Ternary Inverter (PTI), and 3) Negative ternary Inverter (NTI) [4].

Table.3. Truth table of Ternary Inverter

Input (A)	STI Logic Level (Y)	NTI Logic Level (Y)	PTI Logic Level (Y)	STI O/P (Y)
0	2	2	2	0.9 V
1	1	0	2	0.45 V
2	0	0	0	V

2.1 STI INVERTER

Standard Ternary inverter is also called as Simple ternary inverter.



(a) (b)

Fig.3. (a) Structure of STI (b) STI symbol

Standard Ternary Inverter (STI) designed using a PFinFET and NFinFET transistor with three different voltage value i.e. Logic 2 at V_{DD} (0.9V), Logic 0 at Ground (0V) and logic 1 is a middle voltage (i.e. 0.45V) between V_{DD} and Ground [4]. In Fig.2(a), transistor $M1$ is PFinFET and $M2$ is NFinFET. The design requirement can be change by changing the length to width ratio of the PFinFET and NFinFET. The resistance of channels can be change as per the design requirement [4] [5] [6]. The equation for STI is given as,

$$STI = \bar{I}n = 2 - In. \quad (1)$$

When the low voltage (0V) is applied to input of the STI, PFinFET will be in linear region and NFinFET will be in cut-off region. There for output will be high (0.9V) voltage across output terminal. When the middle voltage (0.45V) is applied to input of the STI, both PFinFET and NFinFET will be in saturation region. When the high voltage (0.9V) is applied to input of the STI, PFinFET will be in cut-off region and NFinFET will be in linear region. There for output will be low (0V) voltage across output terminal. Structure and Symbol of STI is shown in Fig.3(a) and Fig.3(b).

2.2 PTI INVERTER

Positive ternary inverter gives high logic value i.e. 2 for two low logic (i.e. 0 and 1) level inputs [7] [8]. Structure of positive ternary inverter is same as STI and NTI structure only width and threshold voltage is different.

When the three values are (0, 1, 2) given to input (*A*) terminal of the PTI, then the values are (2, 2, 0) observed at the output side (*Y*) of the PTI [7] which is mentioned in Table.3 respectively.

2.3 NTI INVERTER

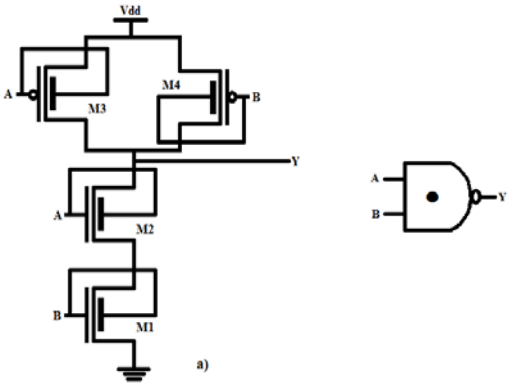
Negative ternary inverter gives low logic value i.e. 0 for two high logic (i.e. 1 and 2) level inputs [7] [8]. Structure of negative ternary inverter is same as STI structure only width and threshold voltage is different.

When the three values are (0, 1, 2) given to input (*A*) terminal of the NTI, then the values are (2, 0, 0) observed at the output side (*Y*) of the NTI [7] which is mentioned in Table.3 respectively.

3. DESIGN OF A STANDARD T-NAND GATE

Structure of Standard Ternary NAND gate is same as binary NAND gate. Structure of two inputs (*A* and *B*) Standard ternary NAND gate is shown in Fig.4(a) and symbol of ST-AND is shown in Fig.4(b). The equation for Standard ternary NAND gate is given as,

$$Y = INV[\text{Min}(A, B,\ldots,In)]. \quad (2)$$



(a) (b)

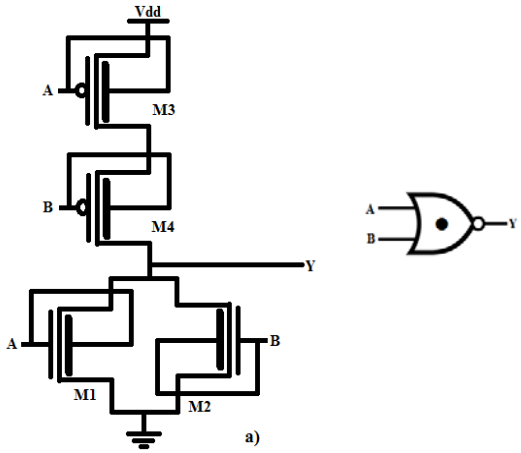
Fig.4. (a) Structure of ST-NAND gate (b) Symbol of ST-NAND gate

Table.4. Truth table of ST-NAND Gate

Input (A)	Input (B)	Output (Y)
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

4. DESIGN OF STANDARD T-NOR GATE

Structure of standard ternary NOR gate is same as binary NOR gate.



(a) (b)

Fig.5. (a) Structure of ST-NOR gate (b) Symbol of ST-NOR gate

Structure of two (*A* and *B*) inputs standard ternary NOR gate is shown in Fig.5(a) and symbol of ST-NOR is shown in Fig.5(b). The equation for standard ternary NOR gate is given as,

$$Y = INV[\text{Max}(A, B,\ldots,In)]. \quad (3)$$

Table.5. Truth table of ST-NOR Gate

Input (A)	Input (B)	Output (Y)
0	0	2
0	1	1
0	2	0
1	0	1
1	1	1
1	2	0
2	0	0
2	1	0
2	2	0

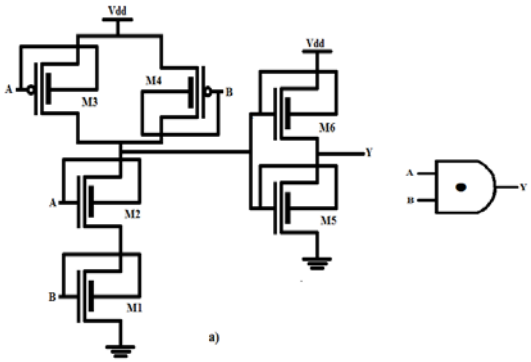
5. DESIGN OF STANDARD T-AND GATE

The basic elements of ternary logic family are STI, ST-NAND and ST-NOR. By using these gates we can further implement ST-AND, ST-OR [4]. Structure of standard ternary AND gate is same as binary AND gate. Structure of two inputs (*A* and *B*) ternary AND gate is shown in Fig.6(a) and symbol of ST-AND gate is shown in Fig.6(b). The equation for standard ternary AND gate is given as,

$$Y = \text{Min}[A, B,\ldots, In]. \quad (4)$$

Table.6. Truth table of ST-AND Gate

Input (A)	Input (B)	Output (Y)
0	0	0
0	1	0
0	2	0
1	0	0
1	1	1
1	2	1
2	0	0
2	1	1
2	2	2



(a) (b)

Fig.6. (a) Structure of ST-AND gate (b) Symbol of ST-AND gate

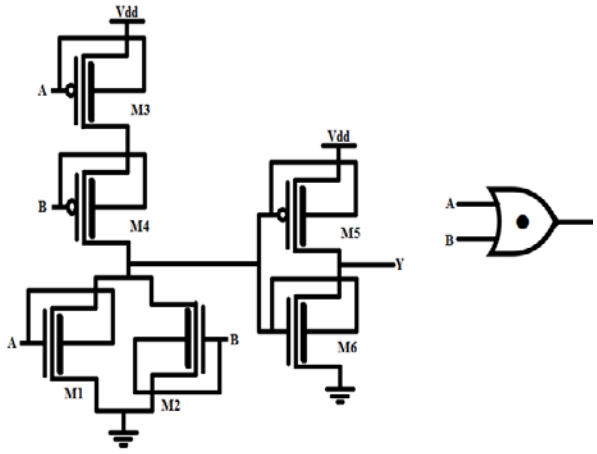
6. DESIGN OF STANDARD T-OR GATE

Structure of standard ternary OR gate is same as binary OR gate. Structure of two inputs (*A* and *B*) ST-OR gate is shown in Fig.7(a) and symbol of ST-OR is shown in Fig.7(b). The equation for standard ternary OR gate is given as,

$$Y = \text{Max}[A, B,\ldots, In]. \quad (5)$$

Table.7. Truth table of ST-OR Gate

Input (A)	Input (B)	Output (Y)
0	0	0
0	1	1
0	2	2
1	0	1
1	1	1
1	2	2
2	0	2
2	1	2
2	2	2



(a) (b)

Fig.7. (a) Structure of ST-OR gate (b) Symbol of ST-OR gate

7. SIMULATION RESULTS

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.02. Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to enter schematics, perform SPICE (Simulation Program with Integrated Circuit Emphasis) simulations, do physical design (i.e. chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks. Although there were many free and powerful SPICE variations, SPICE became a standard of accurate circuit simulator. Tanner EDA is an analog circuit simulator (similar to Berkeley's SPICE-3) capable of performing transient, steady state, and frequency domain analyses. Netlist of the proposed ternary logic gates are designed with help of Berkeley BSIM4 SOI v4.0 library for 32 nm technology using TSPICE.

Truth tables for all gates are verified using W-Edit simulation (Tanner EDA) tool version 13.02 and according to result, Simulation waveform is shown voltage (V) versus time (ns) in below figures.

7.1 STANDARD TERNARY INVERTER

When the three values (0, 1, 2) are given to input (*A*) of the STI, then the values (2, 1, 0) are observed at the output (*Y*) side of the STI [5] which is mentioned in Table.3.

First waveform denotes as input waveform of the STI and second waveform (*A*) denotes as output waveform (*Y*) of STI.

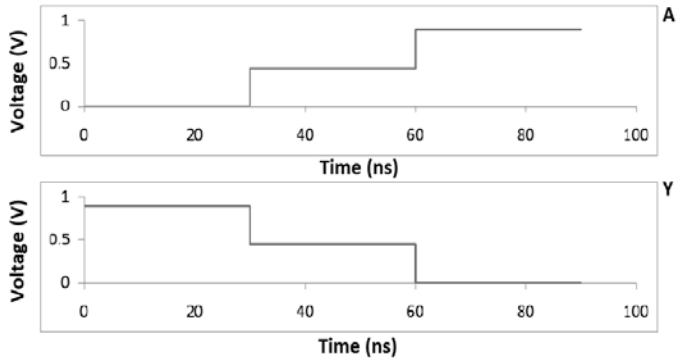


Fig.8. Simulation waveform of STI

7.2 STANDARD TERNARY NAND GATE

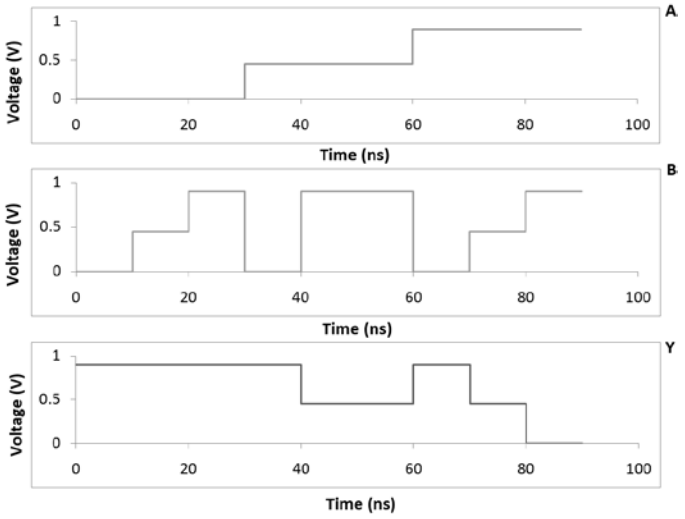


Fig.9. Simulation waveform of ST-NAND gate

The Fig.9 shows the output waveforms for ST-NAND gate. The first two waveforms denote as inputs (*A* and *B*) of the ST-NAND gate and the third waveform indicates output of ST-NAND gate at terminal *Y*. When high value (i.e. 2) is applied at both the input terminal *A* and *B* then low value (i.e. 0) is observed at output terminal (*Y*) of ST-NAND gate form t = 80ns to t = 90ns shown in Fig.9. When low value (i.e. 0) is applied at any one or two input terminal of the ST-NAND gate then high value (i.e. 2) is observed at output terminal (*Y*) of ST-NAND gate from t = 0ns to 40ns and t = 60ns to t = 70ns. Remaining for all condition of the inputs, output will be middle value (i.e. 1) from t = 40ns to 60ns and t = 70ns to 80ns shown in Fig.9.

Truth table of ST-NAND is mentioned in Table.4. The transient characteristic of ST-NAND is shown in Fig.9 for voltage (V) versus time (ns).

7.3 STANDARD TERNARY NOR GATE

The Fig.10 shows the output waveforms for ST-NOR gate. The first two waveform denotes inputs (*A* and *B*) of the ST-NOR gate and the third waveform indicates output of ST-NOR gate at terminal *Y*. When low value (i.e. 0) is applied at both the inputs A and B then high value (i.e. 2) is observed at output terminal (*Y*) of ST-NOR gate from t = 0ns to t = 10ns. When high value (i.e. 2) is applied at any one or two input terminal of the ST-NOR gate then low value (i.e. 0) is observed at output terminal (*Y*) of ST-NOR gate from t = 20ns to 30ns and t = 50ns to 90ns. Remaining for all condition of the inputs, output will be middle value (i.e. 1) from t = 10ns to 20ns and t = 30ns to 50ns shown in Fig.10.

Truth table of ST-NOR gate is mentioned in Table.5. The transient characteristic of ST-NOR is shown in Fig.10 for voltage (V) versus time (ns).

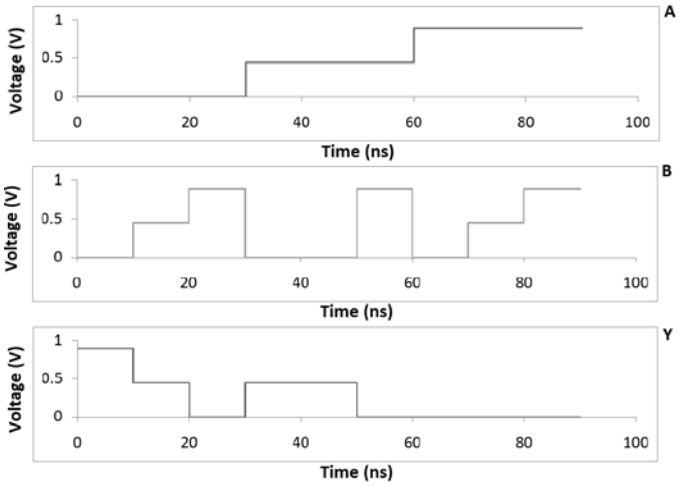


Fig.10. Simulation waveform of ST-NOR gate

7.4 STANDARD TERNARY AND GATE

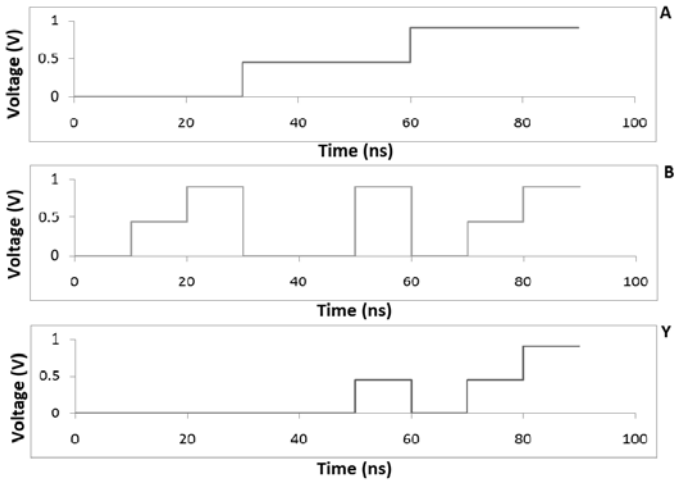


Fig.11. Simulation waveform of ST-AND gate

The Fig.11 shows the output waveforms for ST-AND gate. The first two waveform denotes inputs (*A* and *B*) of the ST-AND gate and the third waveform indicates output of ST-AND gate at terminal *Y*. When high value (i.e. 2) is applied at both the inputs *A* and *B* of the ST-AND gate then high value (i.e. 2) is observed at output terminal (*Y*) of ST-AND gate from t = 80ns to t = 90ns. When low value (i.e. 0) is applied at any one or two input terminal of the ST-AND gate then low value (i.e. 0) is observed at output terminal (*Y*) of ST-AND gate from t = 0ns to 50ns and t = 60ns to 70ns. Remaining for all condition of the inputs, output will be middle value (i.e. 1) from t = 50ns to 60ns and t = 70ns to 80ns.

Truth table of ST-AND is mentioned in Table.6. The transient characteristic of ST-AND is shown in Fig.11 for voltage (V) versus time (ns).

7.5 STANDARD TERNARY OR GATE

The Fig.12 shows the output waveforms for ST-OR gate. The first two waveform denotes inputs (*A* and *B*) of the ST-OR gate and the third waveform indicates output of ST-OR gate at terminal *Y*. When low value (i.e. 0) is applied at both the inputs *A* and *B* of the ST-OR gate then low value (i.e. 0) is observed at output terminal (Y) of ST-OR gate from t = 0ns to t = 10ns. When high value (i.e. 2) is applied at any one or two input terminal of the ST-OR gate then high value (i.e. 2) is observed at output terminal (*Y*) of ST-OR gate from t = 20ns to 30ns and t = 40ns to 90ns. Remaining for all condition of the inputs, output will be middle value (i.e. 1) from t = 10ns to 20ns and t = 30ns to 40ns.

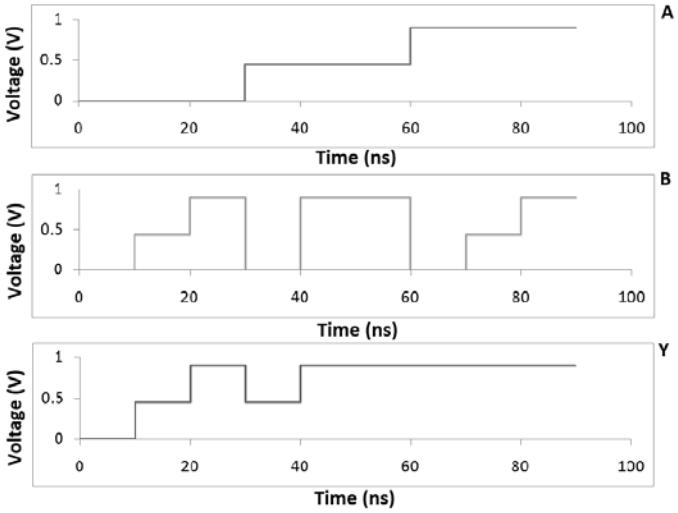


Fig.12. Simulation waveform of ST-OR gate

Truth table of ST-OR is mentioned in Table.7. The transient characteristic of ST-OR is shown in Fig.12 for Voltage versus Time.

7.6 POWER DISSIPATION

Average Power Dissipation is given by sum of Dynamic power dissipation and Static power dissipation. The equation for Power dissipation is given as,

$$P_{avg} = I_{ds} \times V_{dd} + C_L \times V_{dd} \times f \tag{6}$$

where,

I_{ds} = Drain to Source Current (A)
V_{dd} = Supply Voltage (V)
C_L = Output load capacitance (Farad)
F = Clock frequency (HZ).

The average power dissipation of these ternary gates are calculated for the maximum output voltage swing [4]. The designs are proposed with the minimum transistor count thereby reducing the overall power dissipation and reducing the transition times [4].

The Sub threshold leakage current is also known as Drain to source leakage current and is much larger than other leakage currents. The drain to source leakage current is given as,

$$I_{DS} = K\left\{1 - e^{-\left(\frac{V_{DS}}{VT}\right)}\right\} e^{-\left(\frac{V_{GS}-VT+\eta V_{DS}}{\eta VT}\right)} \tag{7}$$

where,

η = DIBL Coefficient
V_T = Threshold Voltage
V_{GS} = Gate to Source Voltage
V_{DS} = Drain to Source Voltage.

Table.8. Power Consumption of Proposed Gates

Sl. No.	Gates	Power Consumption (nW)
1	STI	3.435
2	ST-NAND	8.73
3	ST-NOR	13.49
4	ST-AND	15.63
5	ST-OR	20.77

Table.8 reports the power dissipation of STI, ST-NAND, STNOR, ST-AND and ST-OR gates respectively.

7.7 POWER DELAY PRODUCT

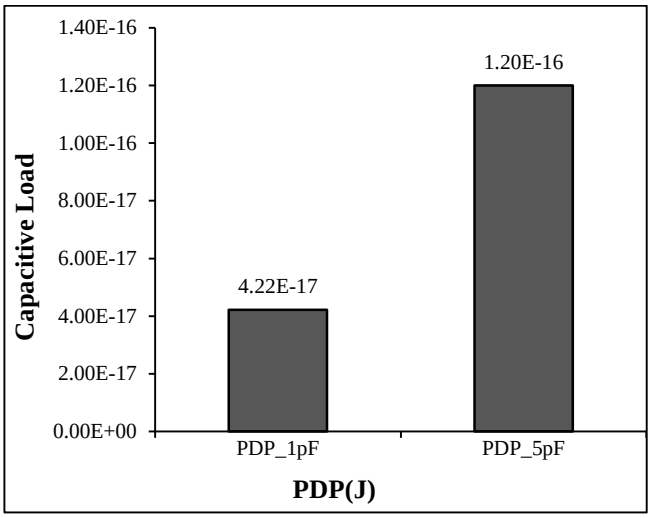


Fig.13. PDP of STI for different capacitive load

The PDP is the product of average power dissipation and propagation delays. Graph of power delay product for STI, ST-NAND gate, ST-NOR gate, ST-AND gate and ST-OR gate is shown in Fig.13, Fig.14, Fig.15, Fig.16 and Fig.17 respectively.

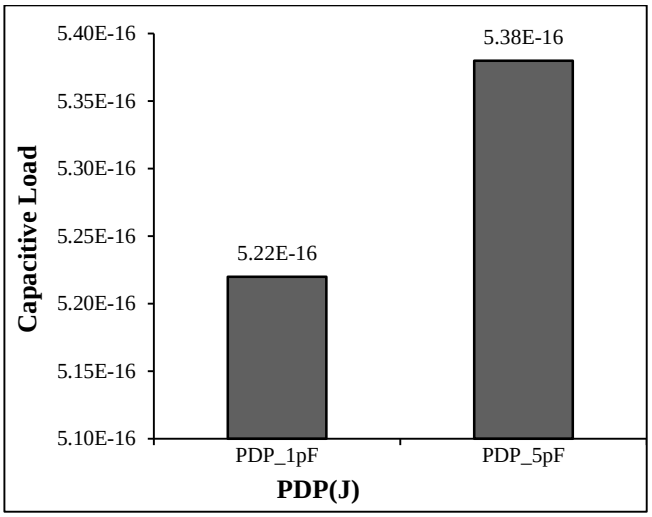


Fig.14. PDP of ST-NAND Gate for different capacitive load

A comparison of the circuit elements used by the researchers is presents in the Table.9. The proposed design has achieved good reduction in the circuit element count [9]. This reduction will further be more prominent when building ternary combinational and sequential circuits [9].

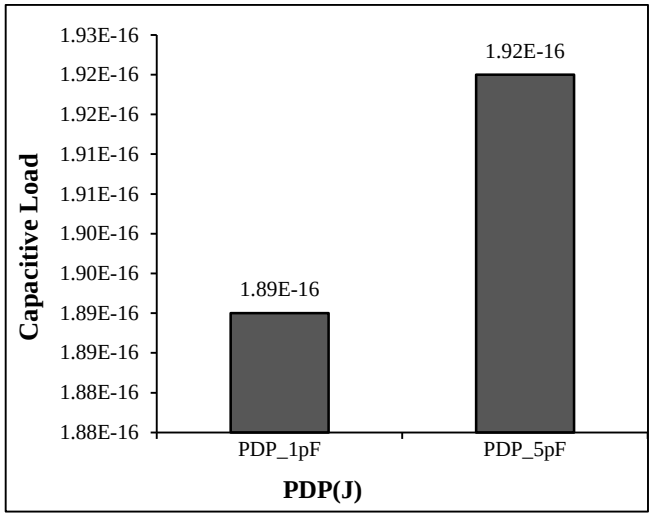


Fig.15. PDP of ST-NOR Gate for different capacitive load

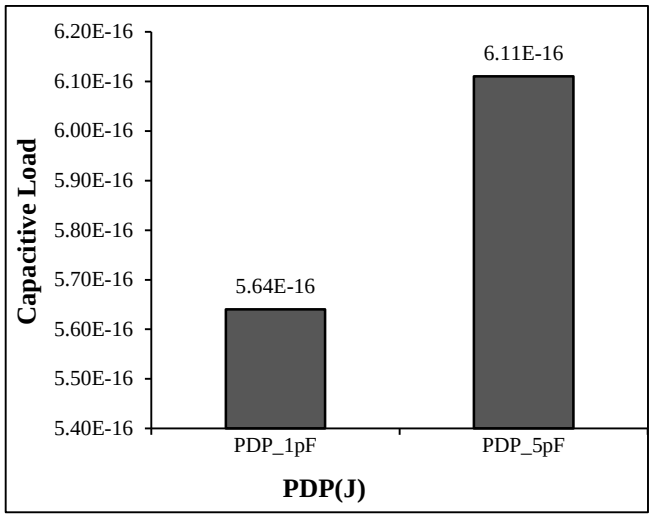


Fig.16. PDP of ST-AND Gate for different capacitive load

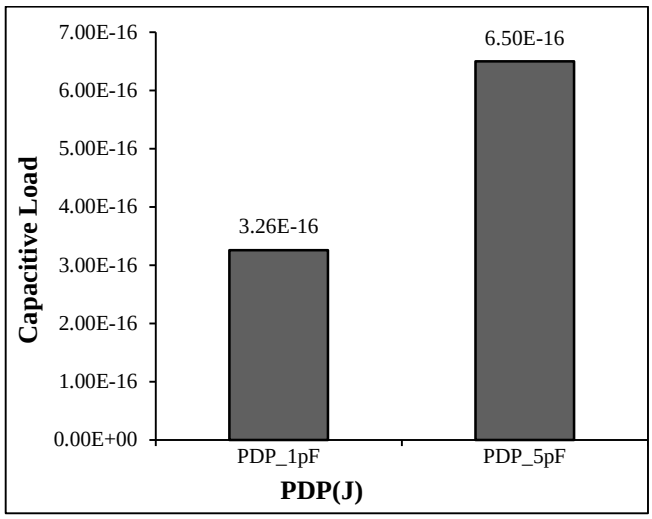


Fig.17. PDP of ST-OR Gate for different capacitive load

Table.9. Comparison of circuit elements

Sl. No.	Ternary Circuits	Different types of MOSFET		
		CNTFET Ref [11]	QDGFET Ref [12]	Proposed design (FinFET)
1	T-INV (STI)	06	03	02
2	ST-NAND	10	04	04
3	ST-NOR	10	04	04
4	ST-AND	16	07	06
5	ST-OR	16	07	06

8. CONCLUSION

This paper proposes a novel FinFET based approach for the realization of the ternary gates. This proposed design shows good reduction in the circuit element count compare to Carbon Nanotube Field-Effect Transistor (CNTFET) and Quantum Dot Gate Field-Effect Transistor (QDGFET). This reduction will further be more prominent when building ternary sequential and combinational circuits. Power consumption for STI, ST-NAND, ST-NOR, ST-AND and ST-OR gates are listed in Table.8 at 32nm technology. Power delay product for STI, ST-NAND, ST-NOR, ST-AND and ST-OR gates are calculated for different capacitive load.

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